V-by-One HS Tx/Rx IP

High-speed serial interface compliant with V-by-One HS standard

Overview

V-by-One HS Tx/Rx IP is an IP to achieve V-by-One HS high-speed video interface technology. V-by-One HS is a standard for next-generation high-speed interface technology developed by THine Electronics for image and video equipment requiring higher frame rates and higher resolutions. Implementing the V-by-One HS Tx/Rx IP in Intel FPGA reduces the number of signals compared with conventional LVDS interfaces, which greatly reduces product cost.

Features

- Achieves 4-Gbps maximum transmission rate per lane (however, depends on the FPGA used)
- Supports custom video formats as well as VESA, SMPTE, and other standardized formats
- Supports flexible multi-lane designs in accordance with user's total transmission rate requirement
- Self-check function (FieldBET) to test connectivity between transmitter and receiver IPs

Specifications

	Transmitter IP	Receiver IP
Lane	1 to 32	
Pixel Data	24, 32, 40 bit	
Self Test Function	FieldBET Pattern Generator	FieldBET Pattern Checker

Supported Devices

- Cyclone® IV GX
- Cyclone V GX/GT
- Cyclone 10 GX
- Arria® II GX
- Arria V GX
- Arria 10 GX
- Stratix® IV GX
- Stratix V GX

(* Please contact Macnica sales department about other devices.)

Deliverables

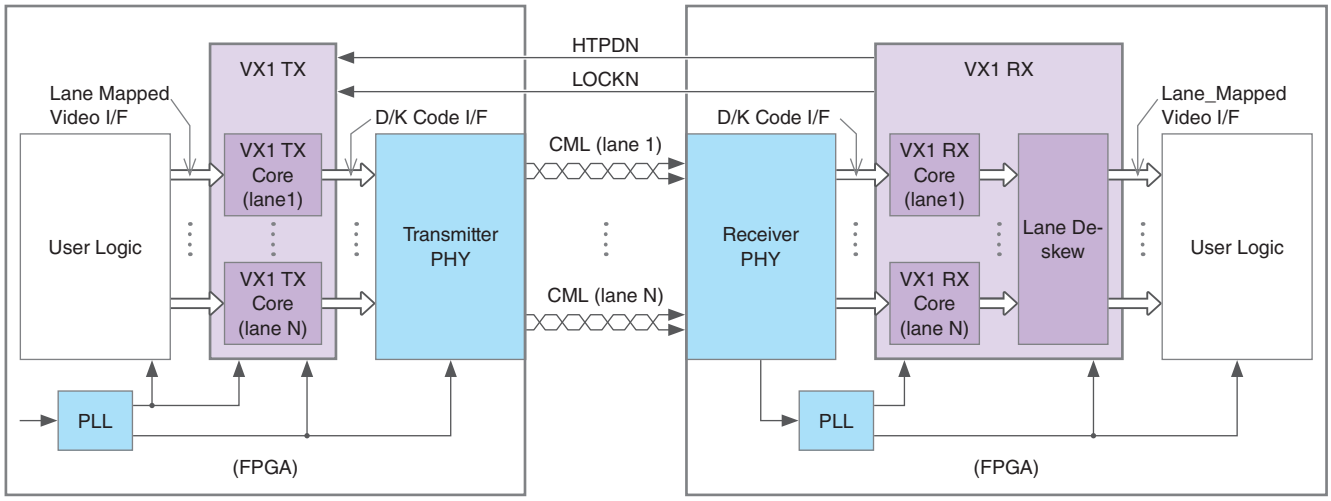
- Encrypted RTL (Verilog HDL)
- Reference design
- Simulation environment (For ModelSim)
- User's manual
- Reference design user's guide

Device Resource Utilization

IP	Lane	Cyclone IV GX			Arria II GX			Stratix IV GX					
		LE	Register	Block Memory	ALUT	Register	Block Memory	ALUT	Register	Block Memory			
TX	2	3,946	2,782	0	1,933	2,782	0	1,933	2,782	0			
RX	2	6,477	4,949	0	2,574	4,949	0	2,574	4,949	0			
IP	Lane	Cyclone V GX			Arria V GX			Stratix V GX			Arria 10 GX		
		ALM	Register	Block Memory	ALM	Register	Block Memory	ALM	Register	Block Memory	ALM	Register	Block Memory
TX	2	1,598	2,977	0	1,603	2,964	0	1,635	2,959	0	1,674	2,976	0
RX	2	2,273	5,416	0	2,274	5,377	0	2,259	5,351	0	2,528	5,218	0

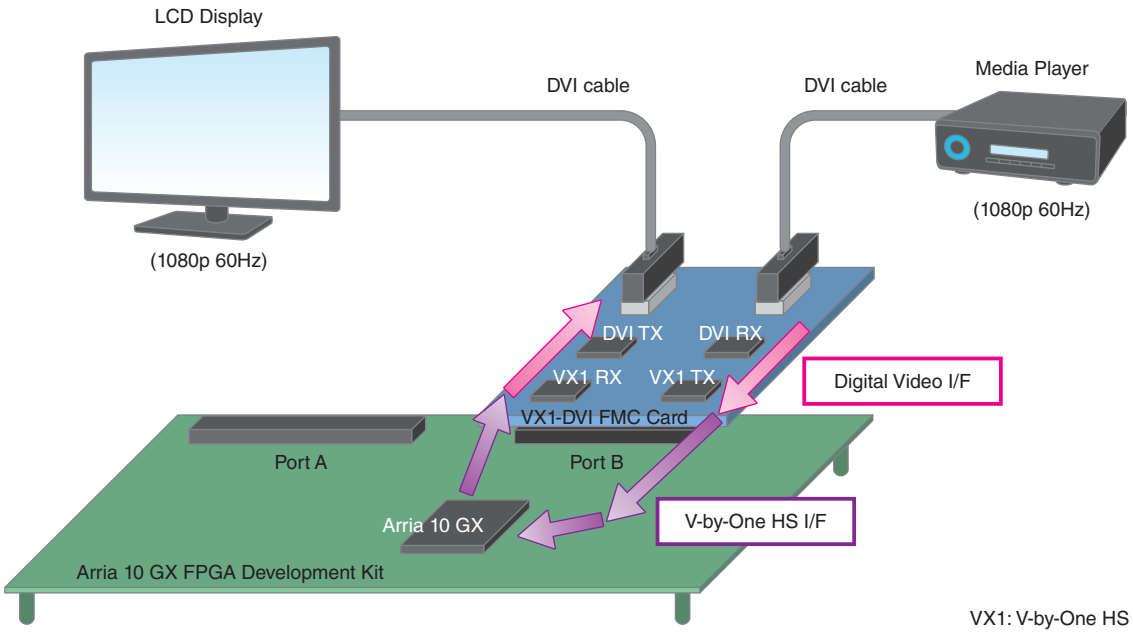
* The values in the above table are based on an implementation example. There may be some variation depending on the user's system configuration.

Configuration Diagram



VX1: V-by-One HS

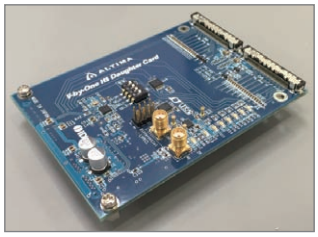
Evaluation Environment



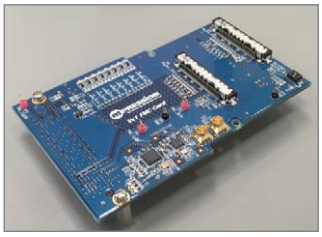
VX1: V-by-One HS

Category	Product Name	Vendor
Main Board	Arria 10 GX FPGA Development Kit	Intel
Daughter Card	V-by-One HS DVI FMC Card	Mpression

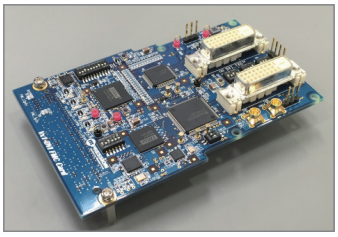
Evaluation Board



V-by-One HS HSMC Card (8-lane)



V-by-One HS FMC Card (16-lane)



V-by-One HS DVI FMC Card