USB3 Vision Device IP Package

High-speed image data transfer complying with USB3 Vision standard

Overview

The USB3 Vision Device IP Package is an IP package to transfer image data complying with USB3 Vision standard. The IP transmits image data from the image sensor to the host computer in real time. High-speed transmission is possible because of USB 3.0 adoption for the communication interface. In addition, any commercially available GenICam compatible applications can control the IP because of its GenICam compliance.
Perfect for high-resolution, high-reliability machine vision cameras, medical imaging systems, and other applications that demand maximized USB 3.0 performance.

Features

- Compliant with USB3 Vision Standard Version 1.01.
- Reference XML file containing camera description based on EMVA GenICam Standard Version 3.0.1 is packaged. Users can start evaluation by using their third-party GenICam applications immediately after purchase.
- USB3 Vision Compliant, Certified by AIA with Logo
- Interoperability qualified with various GenICam application vendors
- Effective transfer rate is >2.9Gbps

Specifications

- Compliant with USB3 Vision Standard Version 1.01
- Compliant with EMVA GenICam Standard Version 3.0.1
- Image data (RAW, YUV, RGB, etc.), Chunk data transfer, Event support

Supported Devices

- Cyclone V + Cypress EZ-USB® FX3™

(* Please contact Macnica sales department about other devices.)

Deliverables

- Encrypted RTL (Verilog HDL)
- Device FW Library for Nios II processor
- USB 3.0 Protocol Stack “USBDmAcs™” for Cypress EZ-USB FX3
- Reference environment (sample hardware design, firmware application, XML file)
- User’s manual

(* Please contact Macnica sales department about other deliverables.)

Device Resource Utilization

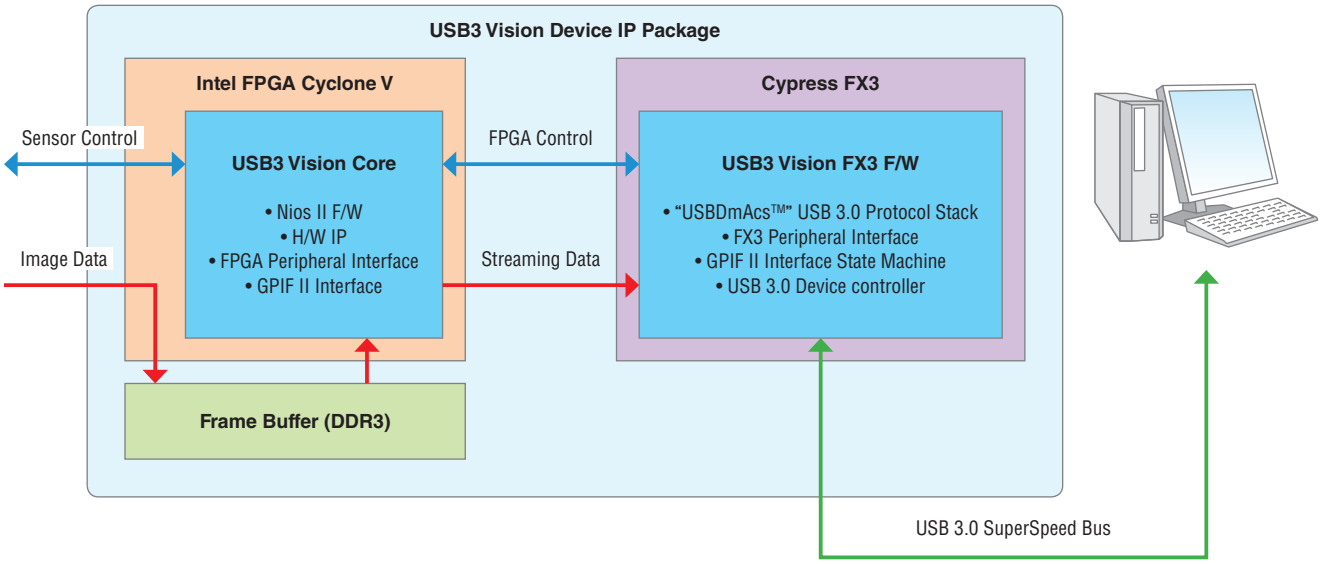
Device	Implementation	GPIF-II IF Data Bus Width	Resource				
			ALMs	Registers	Block Memory (M10Ks)	DSP Blocks	Pins
Cyclone V	IP	16bit	3,136	7,289*2	14	0	-
		32bit	3,137	7,228*2	14	0	-
	Reference Design*1 (IP + Peripherals)	16bit	14,748	28,611	278	5	147
		32bit	14,803	28,490	278	5	163

* The values in the above table are based on an implementation example. There may be some variation depending on the user’s system configuration.

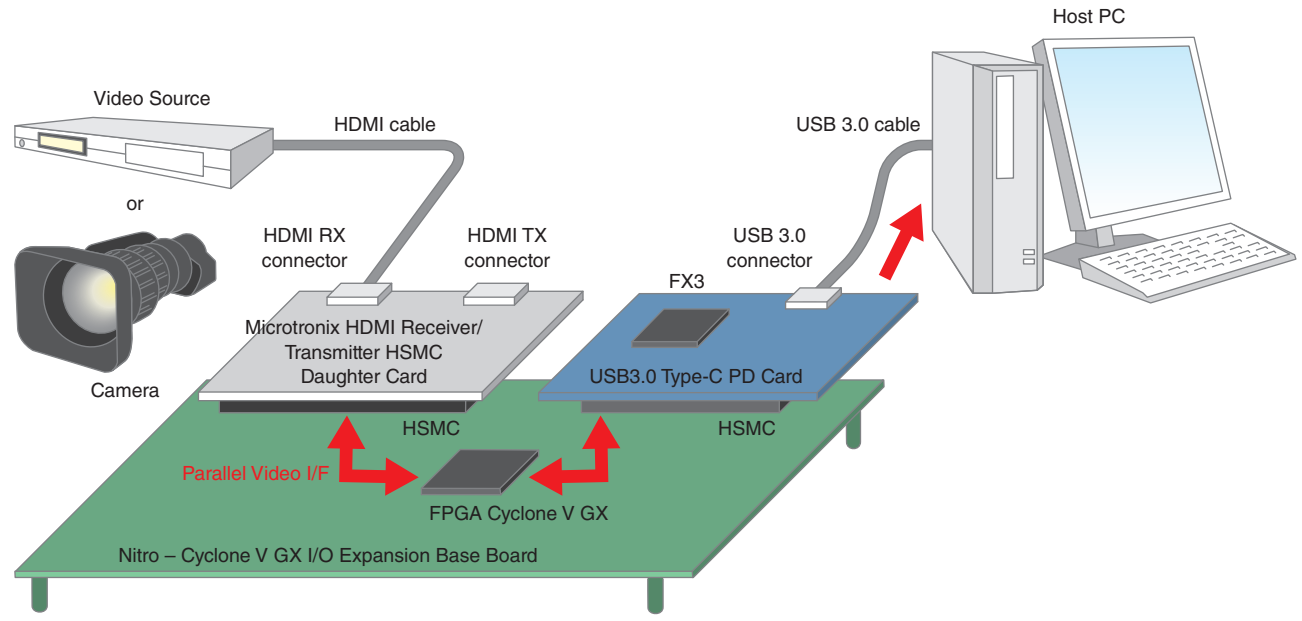
*1: Includes not only IP but also NiosII, DDR3 SDRAM Controller, etc.

*2: IP with 16bit data bus utilizes more resources than IP with 32bit bus because of design specification.

System Block Diagram



Evaluation Environment



Category	Product Name	Vendor
Base Board	Nitro – Cyclone V GX I/O Expansion Base Board	Mpression
Daughter Card	USB3.0 Type-C PD Card	Mpression
Daughter Card	HDMI Receiver/Transmitter HSMC Daughter Card (Option)	Microtronix