SLVS-EC Rx IP

Next generation Sony CMOS image sensor interface

Overview

SLVS-EC Rx IP provides SLVS-EC interface for Intel FPGA to receive image sensor data.
SLVS-EC is Sony's upcoming high-speed interface for next-generation high-resolution CMOS image sensors.
This standard is tolerant of lane-to-lane skew because of embedded clock technology, so that it makes a board level design very easy in terms of high-speed and long distance transmission.

Features

- Compliant with SLVS-EC Specification Version 1.2
- Supports various functions defined by the SLVS-EC Link layer (Intel PCS/PMA is used as Physical layer)
- Supports Byte-to-Pixel conversion for various lane-configurations
- Supports Header analysis and Payload error detection

Specifications

Function	Description
Number of Lanes	1, 2, 4, 6, 8
Baud Grade	1, 2
Bit per Pixel	8, 10, 12, 14
CRC	Limited*
ECC	Supported
Embedded Data	Supported
Dynamic Mode Change	Supported
Multiple Stream	If needed

- The operating frequency may not be achievable depending on the speed grade, number of lanes, and other factors of the FPGA used.

(* Please contact Macnica sales department about limitations.)

Supported Devices

- Cyclone V GX
- Cyclone 10 GX
- Arria 10 GX

(* Please contact Macnica sales department about other devices.)

Deliverables

- Encrypted RTL (Verilog HDL)
- Reference design
- Simulation environment (For ModelSim)
- User's manual, Reference manual, Simulation manual

Device Resource Utilization

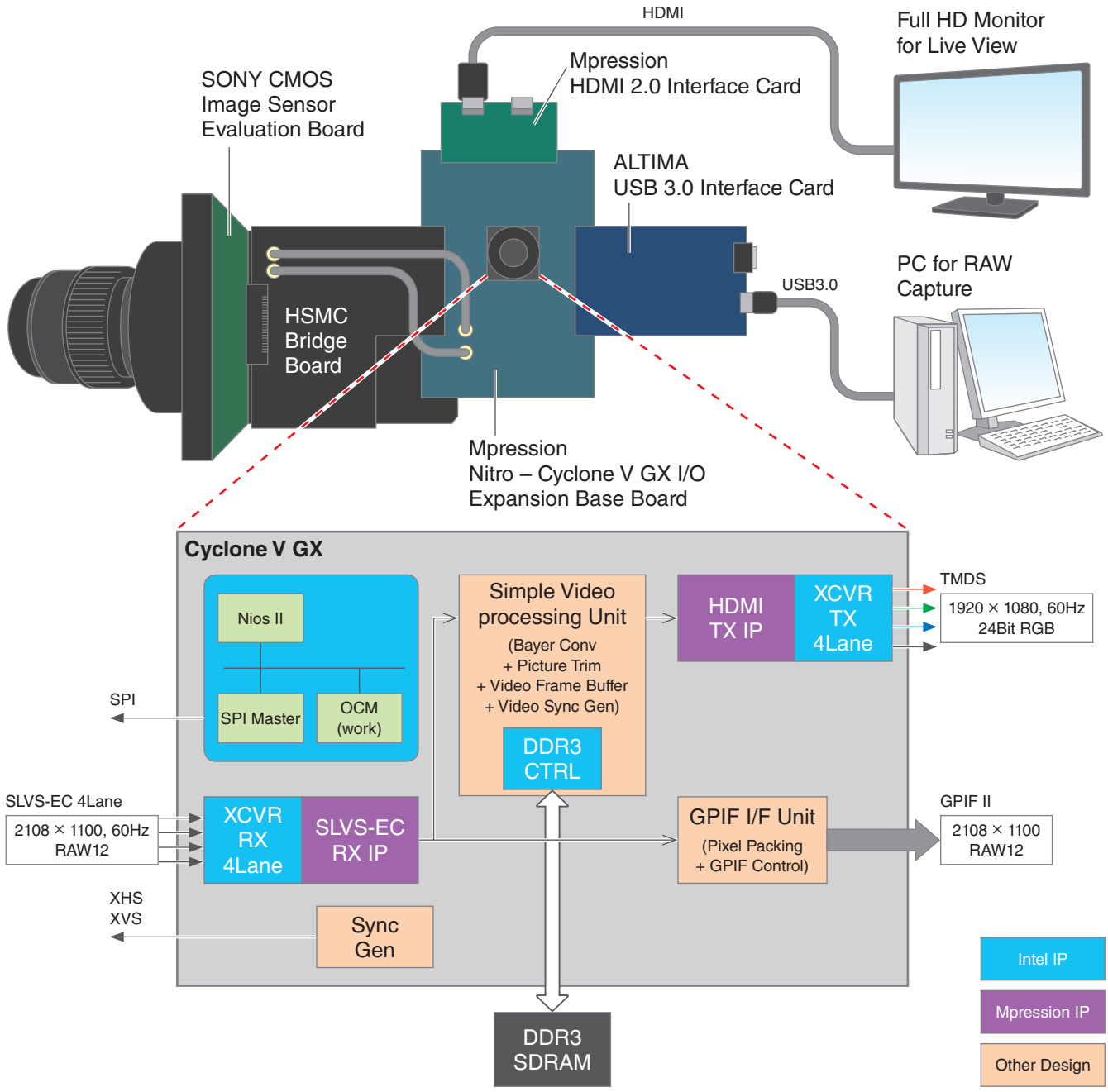
Resource Utilization for 8lane full configuration (including both Transceiver and IP)

Items	Cyclone V GX		Arria 10 GX	
	w/o ECC	w/ECC	w/o ECC	w/ECC
ALMs	4,711	8,242	3,930	7,555
Total Registers	4,328	6,664	3,778	6,079
Total block memory bits	4,096	13,312	2,560	11,776

* The above values are estimated resource utilization of IPs and Transceivers for a full 8 lane-configuration. They may vary depending on your system configuration.

Demo Environment

Data output from Sony CMOS image sensor via SLVS-EC is received by the FPGA.
The FPGA outputs RAW still image to USB3.0 and live video image to HDMI respectively.
In addition to SLVS-EC Rx IP, another Mpression family IP, “HDMI 2.0 Tx IP” is also used in this demonstration.



* This design is not included in the deliverables..

Other

- Please contact Macnica sales department about electrical characterization of Intel FPGA devices regarding SLVS-EC specifications.