IEEE1588 Protocol Stack IP Package

Time synchronization complying with IEEE1588 standard

Overview

IEEE1588 Protocol Stack IP Package complies with IEEE1588 standard and achieves high precision time synchronization with accuracy of 100 nanoseconds or lower. In addition to IEEE1588-2008 compliance, this package is also compliant with SMPTE2059 which is a profile for broadcast equipment. IEEE1588 is a standard for time synchronization scheme between network-connected devices.

Features

- Achieves time synchronization with accuracy of 100 nanoseconds or lower
- Compliant with SMPTE2059 profile in addition to the default PTP profile defined by IEEE1588 standard
- Supports not only a hardware compensation but also a software digital compensation for its frequency compensation mechanism.
- Easy migration to a target hardware, UDP/IP protocol stack, and OS

Specifications

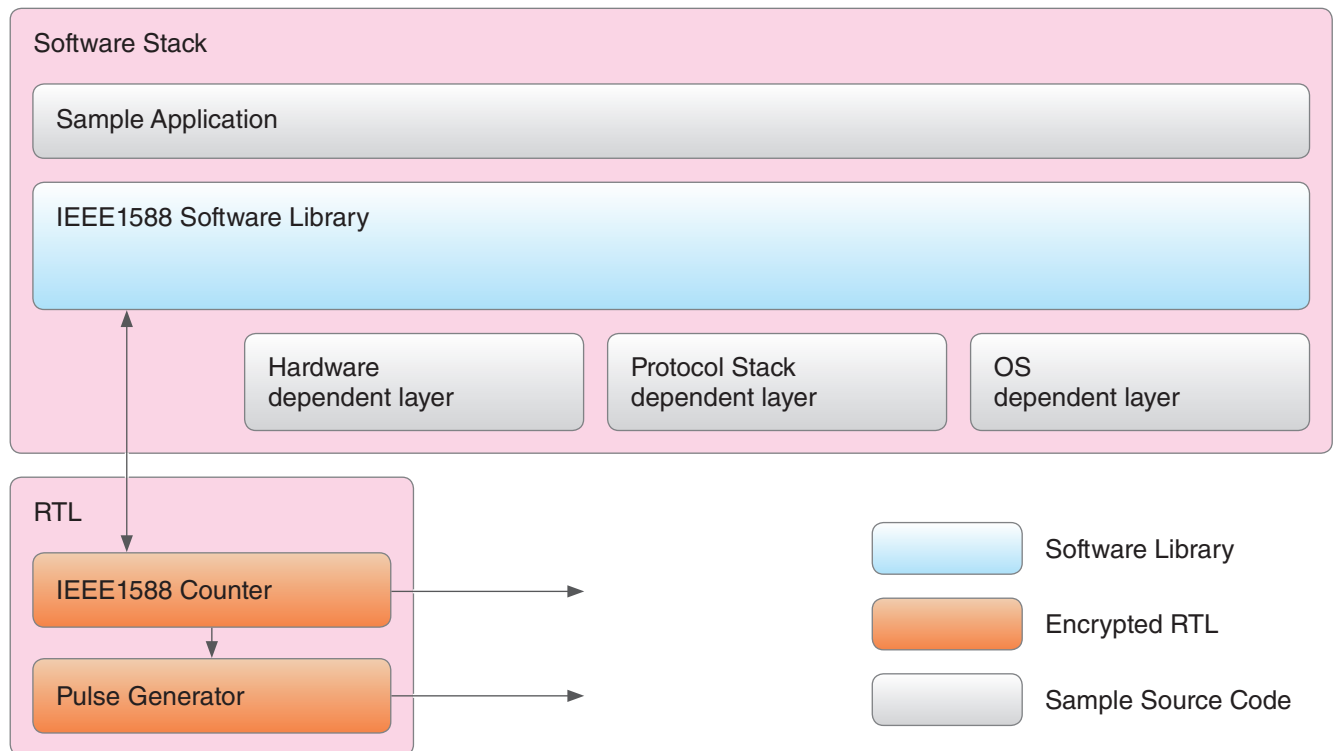|	
PTP Version	PTP Version 2
Clock Type	Ordinary Clock (Slave)
	Ordinary Clock (Master)
Supported Profiles	Delay Request-Response Default PTP profile
	Peer-to-Peer Default PTP profile
	SMPTE2059 profile
Synchronization Message	Two Step
	One Step
Delay Mechanism	End to End
	Peer to Peer
Compensation Mechanism	Phase Compensation
	Frequency Compensation (both hardware compensation and software compensation)

Supported Devices

- Cyclone III/V
- Marvell 88E1512P

(* Please contact Macnica sales department about other devices.)

Deliverables

- Software library
- Encrypted RTL (Verilog HDL)
- Sample software
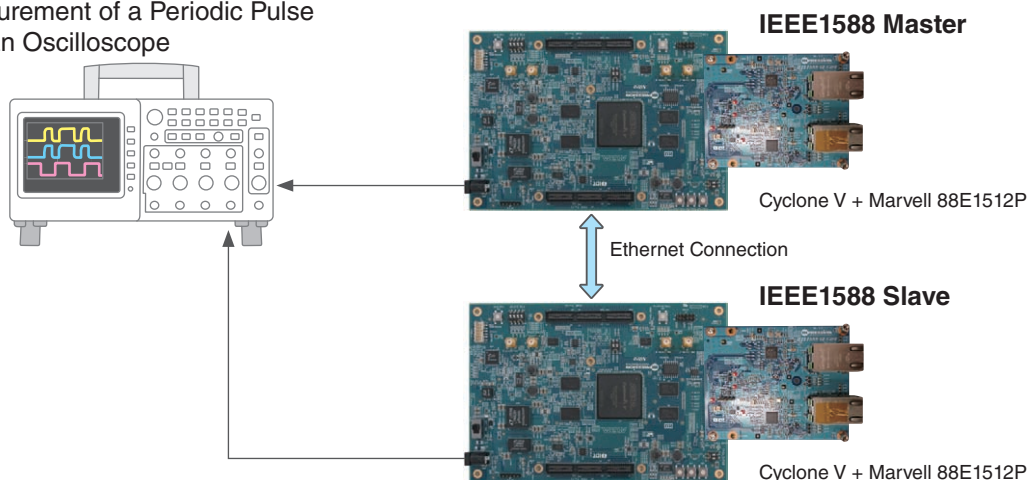- User's manual, Reference manual

Block Diagram

Software Stack

Sample Application

IEEE1588 Software Library

| Hardware dependent layer | Protocol Stack dependent layer | OS dependent layer |

RTL

IEEE1588 Counter

Pulse Generator

Software Library

Encrypted RTL

Sample Source Code

- When operating as a master device, the IEEE1588 software library distributes PTP packets with the value of IEEE1588 counter implemented in RTL.
- When operating as a slave device, the IEEE1588 software library synchronizes the value of IEEE1588 counter with the master device based on the PTP packet information received from the master. The synchronization accuracy is less than 100 nanoseconds.
- A pulse generator implemented in RTL outputs various pulses, such as arbitrary periodic pulses, V-SYNC (video synchronization signals), etc. in accordance with the value of IEEE1588 counter synchronized to the master device
- Functions dependent on user's development environment such as hardware dependent layer are cut out as software layers and it makes easy migration to any target environment.

Evaluation Environment

Measurement of a Periodic Pulse with an Oscilloscope

IEEE1588 Master

Cyclone V + Marvell 88E1512P

Ethernet Connection

IEEE1588 Slave

Cyclone V + Marvell 88E1512P

Category	Product Name	Vendor
Base Board	Nitro – Cyclone V GX I/O Expansion Base Board	Mpression
Daughter Card	IEEE1588 GE Card	Mpression