# HDMI 2.0 Tx/Rx IP

Enables High speed interface compliant with HDMI 2.0 standard

# Overview

HDMI 2.0 Tx/Rx IP provides transmit/receive functions of HDMI 2.0 standard for Intel FPGA. Its maximum transfer rate is 18 Gbps enabling to transmit and receive up to RGB 24 bit 4k2k@60p video. Users can bring their HDMI 2.0 compliant products to market very quickly and easily.

#### Features

- Enables HDMI 2.0 transmission and reception with Intel FPGA
- 18 Gbps maximum transfer rate, supports RGB 24 bit 4k2k@60p transmit and receive (however, depends on the FPGA used)
- HDMI operation confirmed by the third-party compliance test.

#### **Specifications**

- Supports DVI Mode
- Supports Deep Color (30 bit/36 bit/48 bit) Mode
- Supports Display Data Channel (DDC), Status and Control Data Channel (SCDC) control
- Supports Hot Plug Detect, +5V Power Drive control
- Supports Audio

### Supported Devices

- Cyclone V GX (Transfer Rate Limited)
- Cyclone 10 GX
- Arria V GX (Transfer Rate Limited)
- Arria 10 GX

(\* Please contact Macnica sales department about other devices.)

- \*1: The function below is not supported. Content Protection
- \*2: The functions below require to be provided outside of the IP.
  Consumer Electronics Control (CEC)
  HDMI Ethernet and Audio Return Channel (HEAC)

#### Deliverables

- Encrypted RTL (Verilog HDL)
- Reference design
- Simulation environment (For ModelSim)
- User's manual, Reference manual, Simulation manual

## **Device Resource Utilization**

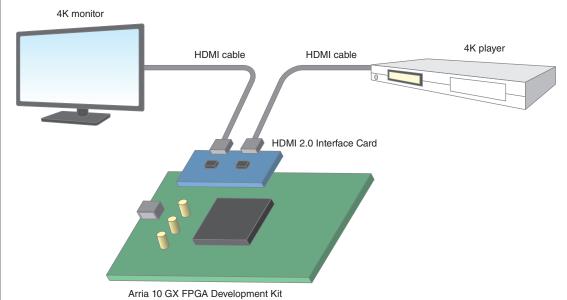
		Symbolo		Resource		
Direction	Device	Symbols per Clock	ALMs	RegisterBlock Memory (M20K or M10k)3,56094,026213,56194,011223,48794,603155,22177,996105,21678,05410	DSP Block	
тх	Cyclone V GX	2	1,808.0	3,560	9	0
		4	2,578.0	4,026	21	0
	Arria V GX	2	1,887.0	3,561	9	0
		4	2,715.0	4,011	22	0
	Arria 10 GX	2	1,939.0	3,487	9	0
		4	2,672.0	4,603	15	0
RX	Cyclone V GX	2	3,469.0	5,221	7	0
		4	5,690.0	7,996	10	0
	Arria V GX	2	3,453.0	5,216	7	0
		4	5,710.0	8,054	10	0
	Arria 10 GX	2	3,447.0	5,072	7	0
		4	5,728.0	7,821	10	0

\* The values in the above table are based on an implementation example. There may be some variation depending on the user's system configuration.



# **Evaluation Environment**

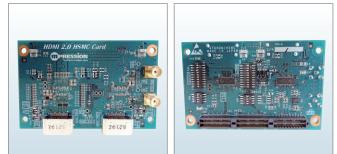
Video from a 4K player is received by the receiver IP, and the video is output to a 4K monitor from the transmitter IP.



Category	Product Name	Vendor
Base Board	Arria 10 GX FPGA Development Kit	Intel
Daughter Card	HDMI 2.0 Interface Card	Mpression



HDMI 2.0 Interface Card FMC Version



HDMI 2.0 Interface Card HSMC Version