Σ-LINK Master IP

Communication master for Yaskawa Electric motor encoders

Overview

Σ-LINK Master IP is an IP that supports Σ-LINK based on Yaskawa Electric's Encoder communication protocol. This IP transmits data collected from the products that support Σ-LINK to CPU.

Features

- Collects data from products that support Σ-LINK by its serial communication link
- Supports Avalon® and APB bus for communication between FPGA and CPU collecting and processing data
- Supports CPU Interrupt

Supported Devices

- Cyclone V

(* Please contact Macnica sales department about other devices.)

Deliverables

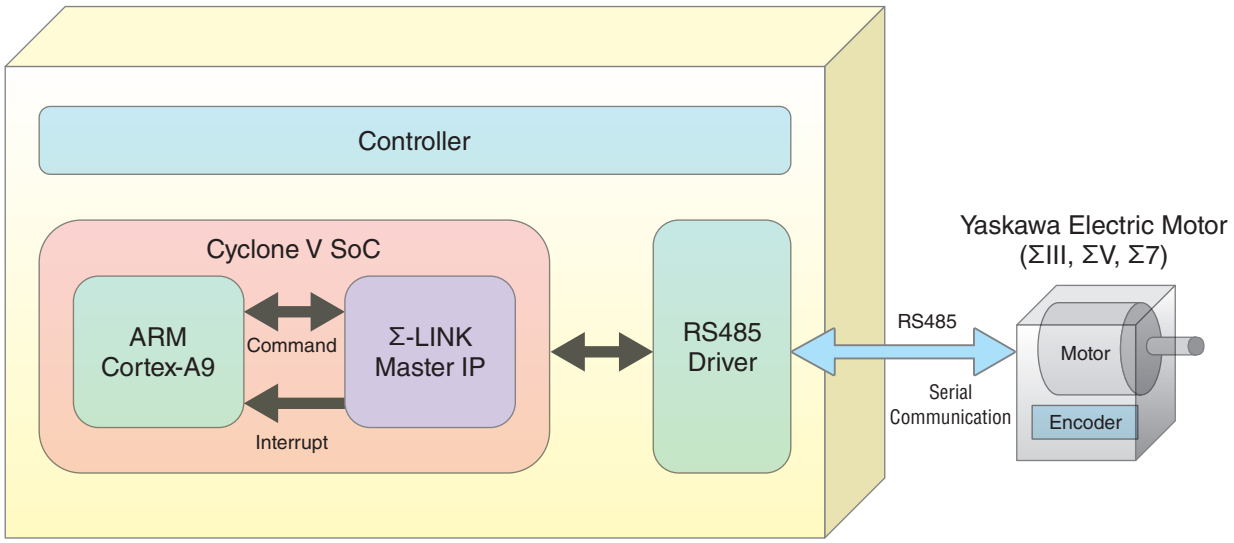
- Encrypted RTL (Verilog HDL)
- Reference design
- Sample driver
- User's manual

Device Resource Utilization

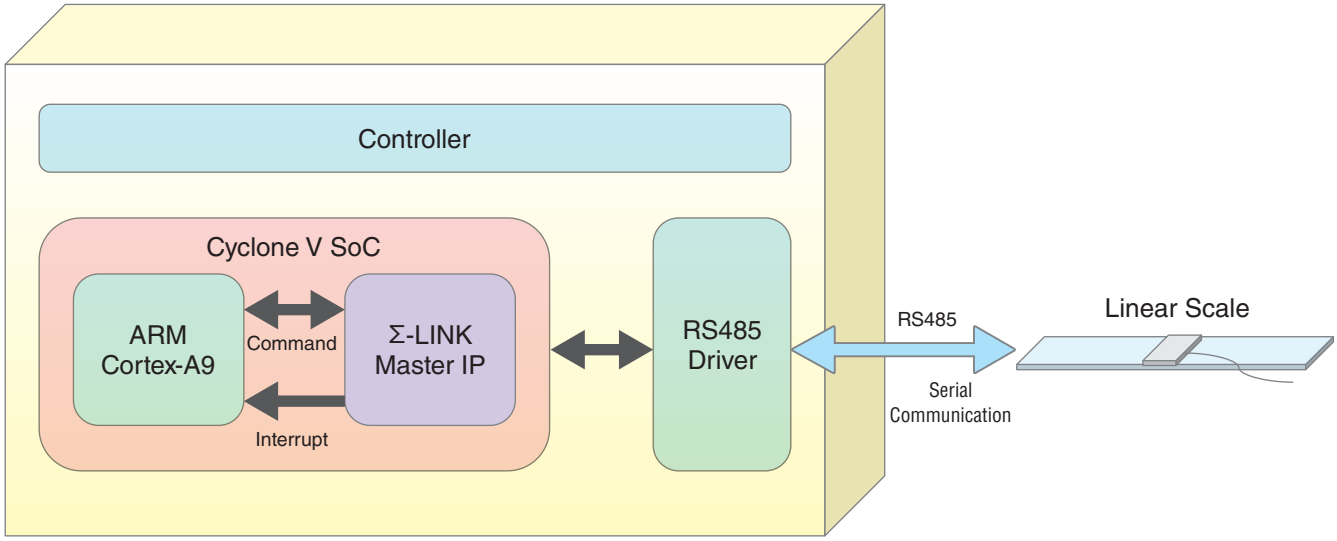
- Cyclone V
  Logic utilization: 3,000 ALMs

Example System Configurations

Example System Configuration 1



Example System Configuration 2



- Transmits data collected from the products that support Σ-LINK to CPU.
- Interrupts to CPU