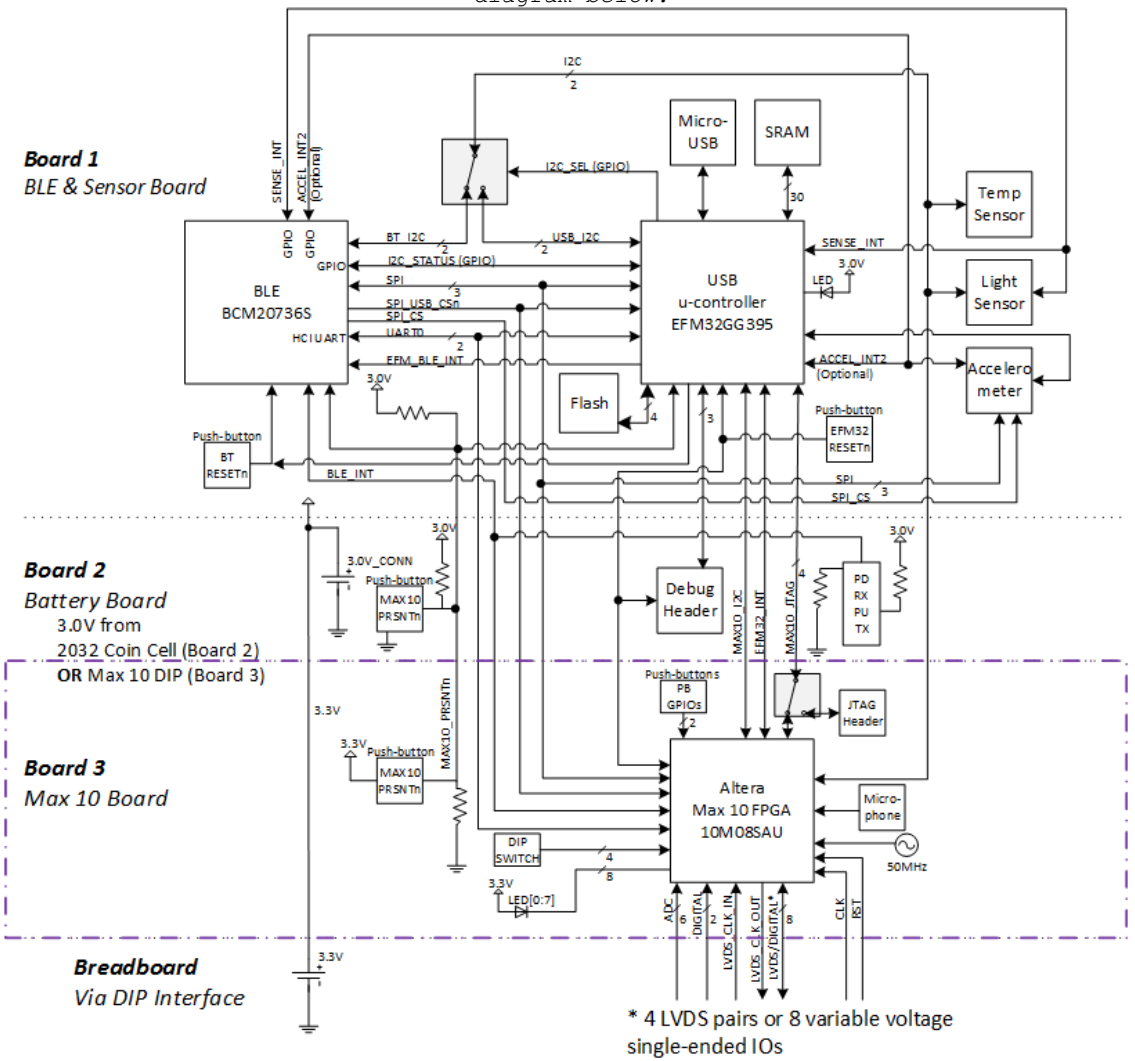
IoT Development Kit
Max 10 Board

This schematic is "Board 3" of the complete demonstration board, shown in the block diagram below.

REV	DATE	PAGES	DESCRIPTION
A0.01	08/28/2014	ALL	Still a lot to do.
A0.02	09/08/2014	ALL	Remove SRAM, update Max 10 pinout, add adj regulator, misc.
A0.03	09/12/2014	1-3	Update block diagram, add microphone and 50MHz clock.
A0.04	09/12/2014	ALL	Update block diagram. Add push-buttons. Add 3.3V power mux.
A0.05	09/16/2014	ALL	Add power block diagram. Change SW1 to U6. Change footprint names for J2. Change J5 to TH part. Update Max 10 VREF pins.
A0.06	09/16/2014	3	Update block diagram. Change J2 pinout so that the pcb footprint can be updated such that pin 1 aligns with the notch in the connector.
A0.07	09/30/2014	3	Add IR LED. Change op-amp to LT6220. Add power muxing for VCCIO_VAR rather than jumper voltage select.
A0.08	10/7/2014	2-3	Add mounting hole symbols for BOM. Add pull-up to op-amp in. DNI LVDS_I_CLK_P/LVDS_I_CLK_N 100-ohm resistor. Update LVDS notes on sheet 2.
A0.09	10/8/2014	2-3	Move IR_LED to pin K10. Change op-amp input pull-up to 10K, not DNI.
A0.10	10/9/2014	3	Add 0603 pull-up and pull-down resistor options to UART_RX.
B1.01	12/10/2014	3	Add Capacitor to Microphone Amp Feedback, Fix IRDA polarity
B1.02	12/12/2014	3-4	Changed Microhpone Gain, and Variable IO Switch Points
B1.03	12/16/2014	4	Change IO Voltage Switch Points
B1.04	01/21/2015	3	Changed R45 to 1K from 10K



* 4 LVDS pairs or 8 variable voltage single-ended IOs

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MAX 10

ANALOG[1:5] still needs to be verified in Quartus.
When using ANAIN1 you cannot use GPIO on banks 1A or 1B.
3.0V/3.3V not recommended (HB) in bank 8 when using ADC. Only 28% of bank 8 will be available for usage. Table 3-4, 3-5.
Disable JTAG when using ADC.

LAYOUT NOTES:
- Route ANALOG[0:5], ANALAG_SIG[1:5], and ANAIN1 signals adjacent to ADC_GND.

U1A

Bank 1A
ANALOG2 C2 — ADC1IN2/DIFFIO_RX_L1_P
ANALOG1 D1 — ADC1IN1/DIFFIO_RX_L1_N
ANALOG4 E4 — ADC1IN4/DIFFIO_RX_L3_P
ANALOG3 E3 — ADC1IN3/DIFFIO_RX_L3_N
ADC1IN6/DIFFIO_RX_L5_P
ADC1IN5/DIFFIO_RX_L5_N
ADC1IN8/DIFFIO_RX_L7_P
ADC1IN7/DIFFIO_RX_L7_N
B1 MIC_ANALOG
C1 ANALOG5
E1
F1

Bank 1B
G4 F4 H3 H2 — DIFFIO_RX_L14_P / DIFFIO_RX_L14_N / DIFFIO_RX_L16_P / DIFFIO_RX_L16_N
TCK/DIFFIO_RX_L11_P
TMS/DIFFIO_RX_L11_N
TDO/DIFFIO_RX_L12_P
TDI/DIFFIO_RX_L12_N
JTAGEN/DIFFIO_RX_L9_P
G2 MAX10_JTAG_TCK
G1 MAX10_JTAG_TMS
F6 MAX10_JTAG_TDO
F5 MAX10_JTAG_TDI
E5 JTAG_EN
3.3V
R51 DNI
R53 DNI

Bank 2
LVDS requires VCCIO=2.5V.
R41 DNI LVDS_I_CLK_P
LVDS_I_CLK_N
H6 G5 H4 H5 N3 N2 L2 — CLK0_P/DIFFIO_RX_L18_P / CLK0_N/DIFFIO_RX_L18_N / CLK1_P/DIFFIO_RX_L20_P / CLK1_N/DIFFIO_RX_L20_N / DPCLK1/DIFFIO_RX_L22_P / DPCLK0/DIFFIO_RX_L22_N / IO_B2
PLL_L_CLKOUT_P/DIFFIO_RX_L27_P
PLL_L_CLKOUT_N/DIFFIO_RX_L27_N
DIFFIO_RX_L19_P / DIFFIO_RX_L19_N / DIFFIO_RX_L21_P / DIFFIO_RX_L21_N / DIFFIO_RX_L28_P / DIFFIO_RX_L28_N
L3 M3 J2 J1 M2 M1 K2 K1

Bank 3
R20 DNI LVDS_O_CLK_P
LVDS_O_CLK_N
R31 DNI LVDS_OUT0_P
LVDS_OUT0_N
L4 L5 K5 M7 N6 K6 J6 K7 J7 — DIFFIO_TX_RX_B1_P / DIFFIO_TX_RX_B1_N / DIFFIO_TX_RX_B3_P / DIFFIO_TX_RX_B3_N / DIFFIO_TX_RX_B5_P / DIFFIO_TX_RX_B5_N / DIFFIO_TX_RX_B7_P / DIFFIO_TX_RX_B7_N / DIFFIO_TX_RX_B9_P / DIFFIO_TX_RX_B9_N
M5 M4 N5 N4 — DIFFIO_RX_B2_P / DIFFIO_RX_B2_N / DIFFIO_RX_B4_P / DIFFIO_RX_B4_N
N12 — IO_B3
DIFFIO_TX_RX_B10_P
DIFFIO_TX_RX_B10_N
DIFFIO_TX_RX_B12_P
DIFFIO_TX_RX_B12_N
DIFFIO_TX_RX_B14_P
DIFFIO_TX_RX_B14_N
DIFFIO_TX_RX_B16_P
DIFFIO_TX_RX_B16_N
M12 LVDS_OUT3_P R22 DNI
M13 LVDS_OUT3_N
L11 LVDS_OUT2_P R33 DNI
M11 LVDS_OUT2_N
K8 LVDS_OUT1_P R40 DNI
J8 LVDS_OUT1_N
L10
M10
LVDS requires VCCIO=2.5V.
DIFFIO_RX_B6_P / DIFFIO_RX_B6_N / DIFFIO_RX_B8_P / DIFFIO_RX_B8_N / DIFFIO_RX_B11_P / DIFFIO_RX_B11_N
N8 N7 M9 M8 N9 N10

LAYOUT NOTES:
- LVDS pairs should be routed as loosely coupled, so that they can also be used as single-ended IO.
- Place LVDS 100-ohm resistors near FPGA.

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U1B

Bank 5
IR_LED K10
LED2 PB1 J12
LED0 L13
DIFFIO_RX_R1_P / DIFFIO_RX_R1_N / DIFFIO_RX_R2_P / DIFFIO_RX_R2_N / DIFFIO_RX_R7_P / DIFFIO_RX_R7_N / IO_B5
J10 K11 L12 K12
DIFFIO_RX_R8_P / DIFFIO_RX_R8_N / DIFFIO_RX_R9_P / DIFFIO_RX_R9_N / DIFFIO_RX_R10_P / DIFFIO_RX_R10_N / DIFFIO_RX_R11_P / DIFFIO_RX_R11_N
J9 H10 J13 H13 H9 H8 G13 G12 — LED3 LED1 LED7 LED4 LED6 LED5

Bank 6
CLK_RST G9
RESET G10
CLK_50MHZ F13
EFM32_INT E13
BLE_INT F9 F10
CLK2_P/DIFFIO_RX_R14_P / CLK2_N/DIFFIO_RX_R14_N / CLK3_P/DIFFIO_RX_R16_P / CLK3_N/DIFFIO_RX_R16_N / DPCLK3/DIFFIO_RX_R26_P / DPCLK2/DIFFIO_RX_R26_N
DIFFIO_RX_R18_P / DIFFIO_RX_R18_N / DIFFIO_RX_R27_P / DIFFIO_RX_R27_N / DIFFIO_RX_R28_P / DIFFIO_RX_R28_N / DIFFIO_RX_R29_P / DIFFIO_RX_R29_N / DIFFIO_RX_R30_P / DIFFIO_RX_R30_N / DIFFIO_RX_R31_P / DIFFIO_RX_R31_N / DIFFIO_RX_R33_P / DIFFIO_RX_R33_N
F12 E12 F8 E9 B12 B11 C12 C11 B13 A12 E10 D9 D12 D11 — DIGITAL12 EFM32_RESETn SPI_SCLK SPI_USB_CSn SPI_MISO UART0_TX SPI_MOSI DIGITAL13 I2C_SDA I2C_SCL MAX10_I2C_SDA UART0_RX

Bank 8
MAX10_I2C_SCL C13
BOOT_SEL D7
nCONFIG E7
nSTATUS C4
CONF_DONE C5
DIPSW1 B10 B9 D8 E8
IO_B6
BOOT_SEL
nCONFIG
nSTATUS/DIFFIO_RX_T24_P
CONF_DONE/DIFFIO_RX_T24_N
DIFFIO_RX_T22_P
CRC_ERROR/DIFFIO_RX_T22_N
DIFFIO_RX_T16_P
DEV_CLRn/DIFFIO_RX_T16_N
DEV_OE/DIFFIO_RX_T18_P
DIFFIO_RX_T18_N
E6 D6
DIFFIO_RX_T14_P / DIFFIO_RX_T14_N / DIFFIO_RX_T15_P / DIFFIO_RX_T15_N / DIFFIO_RX_T17_P / DIFFIO_RX_T17_N / DIFFIO_RX_T19_P / DIFFIO_RX_T19_N / DIFFIO_RX_T20_P / DIFFIO_RX_T20_N / DIFFIO_RX_T21_P / DIFFIO_RX_T21_N / DIFFIO_RX_T23_P / DIFFIO_RX_T23_N / DIFFIO_RX_T25_P / DIFFIO_RX_T26_P / DIFFIO_RX_T26_N
C10 C9 A8 A9 A10 A11 A7 A6 B6 B5 A4 A3 B3 B4 A5 A2 B2 — DIPSW0 DIPSW2

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LED[0:7] 3
DIPSW[0:2] 3
PB[0:1] 3
IR_LED 3
BOOT_SEL 3
CLK_50MHZ 3
MIC_ANALOG_SIG 3

30-Pin Connector to BLE/Sensor Board
EFM32_JTAG_TCK 3
EFM32_JTAG_TMS 3
EFM32_JTAG_TDI 3
EFM32_JTAG_TDO 3
EFM32_RESETn 3
EFM32_INT 3
BLE_INT 3
SPI_SCLK 3
SPI_USB_CSn 3
SPI_MOSI 3
SPI_MISO 3
UART0_TX 3
UART0_RX 3
I2C_SCL 3
I2C_SDA 3
MAX10_I2C_SCL 3
MAX10_I2C_SDA 3

DIP Pins
DIGITAL12 3
DIGITAL13 3
ANALOG0 3
ANALOG_SIG[1:5] 3
RESET 3
CLK_RST 3
LVDS_I_CLK_N 3
LVDS_I_CLK_P 3
LVDS_O_CLK_N 3
LVDS_O_CLK_P 3
LVDS_OUT3_N 3
LVDS_OUT3_P 3
LVDS_OUT2_N 3
LVDS_OUT2_P 3
LVDS_OUT1_N 3
LVDS_OUT1_P 3
LVDS_OUT0_N 3
LVDS_OUT0_P 3

For best LVDS RX performance, the DNI resistors on the LVDS pairs should be populated with a 100 ohm resistors; otherwise, if using the pairs as LVDS, they should be termination on the user's breadboard as close as possible to the DIP pins using 100 ohm resistors.

U1C
Max 10S Power
Single Supply
Core & Periphery 3.0V/3.3V
PLL & ADC 3.0V/3.3V

3.3V — C19 16V 1uF — C16 25V 0.1uF
VCC_ONE F7 G6 G8 H7
3.3V_VCCA — C23 16V 1uF — L4 BEAD 3.3V
VCCA1 D10 VCCA2 D4 VCCA3 K9 VCCA4 K4

3.3V — L3 BEAD — 3.3V_VCCIO1A
VCCIO1A F2 VCCIO1B G3 VREFB1N0/IO H1
VCCIO
VCCIO5 H11 VCCIO5 J11 VREFB5N0/IO K13 — PB0
3.3V
VCCIO2 J3 VCCIO2 K3 VREFB2N0/IO L1
VCCIO6 F11 VCCIO6 G11 VREFB6N0/IO D13
VCCIO_VAR
C8 16V 1uF
VCCIO3 L6 VCCIO3 L7 VCCIO3 L8 VREFB3N0/IO N11
VCCIO8 C6 VCCIO8 C7 VCCIO8 C8 VREFB8N0/IO B7
C17 16V 1uF

GND A1 A13 B8 C3 D5 E11 F3
GND N13 N1 M6 L9 J4 H12 G7

ADC Power Block
2.5V
ADC_VREF D3
REFGND E2
ANAIN1 D2

ANALOG_SIG1 R24 10.0 ANALOG1 C9 1pF 50V
ANALOG_SIG2 R25 10.0 ANALOG2 C10 1pF 50V
ANALOG_SIG3 R26 10.0 ANALOG3 C11 1pF 50V
ANALOG_SIG4 R27 10.0 ANALOG4 C12 1pF 50V
ANALOG_SIG5 R28 10.0 ANALOG5 C13 1pF 50V
MIC_ANALOG_SIG R8 10.0 MIC_ANALOG C3 1pF 50V

LAYOUT NOTES:
- Place RC circuits near Max 10.

ADC_GND ADC_REF
C6 1uF 16V — L5 BEAD — ADC_GND
ADC_GND

Assuming RC is from the connector.
ANAIN1 — C14 1pF 50V — R29 10.0 — ANALOG0
ADC_GND

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Place TCK filter near Max 10.
C20 DNI 25V — R43 DNI — R49 10.0K
C24 0.1uF 25V

U3
VDD 14
D1 IN1 S1A 20 — EFM32_JTAG_TCK
S1B 2 — JTAG_TCK
D2 IN2 S2A 7 — EFM32_JTAG_TMS
S2B 5 — JTAG_TMS
D3 IN3 S3A 11 — EFM32_JTAG_TDO
S3B 13 — JTAG_TDO
D4 IN4 S4A 17 — EFM32_JTAG_TDI
S4B 15 — JTAG_TDI
NC 10
VSS 3
EPAD(VSS) 21
GND 4
ADG788

MAX10_JTAG_TCK 1 JTAG_SEL 19
MAX10_JTAG_TMS 6 JTAG_SEL 8
MAX10_JTAG_TDO 12 JTAG_SEL 9
MAX10_JTAG_TDI 16 JTAG_SEL 18

3.3V — R57 10.0K — R59 10.0K — R48 10.0K

When a USB Blaster cable is plugged in, the JTAG connector pin 2 will be pulled to GND. This will remove control of the JTAG chain from the BLE/Sensor Board.

J2
JTAG_TCK 1
JTAG_TDO 3
JTAG_TMS 5
JTAG_TDI 9
JTAG_SEL 2 4 6 8 10
JTAG HDR 2X5

JTAG_SEL = 0 -> Connect Dx to SxB (JTAG Header)
JTAG_SEL = 1 -> Connect Dx to SxA (BLE/Sensor Board)

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CONNECTOR & IO

MH1 MH_SPACER
MH2 MH_SPACER
MH3 MH_SPACER
MH4 MH_SPACER

3.3V
R2 10.0K MAX10_I2C_SCL
R52 10.0K MAX10_I2C_SDA

3.3V
VIN_3.3V
J1 RECEPTACLE_2X15
I2C_SCL
I2C_SDA
BLE_INT
EFM32_INT
MAX10_I2C_SCL
MAX10_I2C_SDA
EFM32_JTAG_TMS
EFM32_JTAG_TCK
EFM32_JTAG_TDI
UART0_TX
GND
I2C_SCL
I2C_SDA
VIN_MAIN
BLE_INT
EFM32_INT
GND
MAX10_I2C_SCL
MAX10_I2C_SDA
VOUT_MAIN
MAX10_JTAG_TMS
MAX10_JTAG_TCK
GND
MAX10_JTAG_TDI
UART_TX
UART_RX
GND
SPI_SCLK
SPI_CS
VIN_MAIN
SPI_MISO
SPI_MOSI
GND
DBG_SWDIO
DBG_SWO
VOUT_MAIN
DBG_SWCLK
EFM32_RESETn
MAX10_PRSNTn
MAX10_JTAG_TDO
UART0_RX
SPI_SCLK
SPI_USB_CSn
SPI_MISO
SPI_MOSI
DBG_SWDIO
DBG_SWO
DBG_SWCLK
EFM32_RESETn
MAX10_PRSNTn
EFM32_JTAG_TDO
R56 DNI
R55 10.0K, 0603
VIN_3.3V
3.3V
S3 PB-SPST-NO
R45 1.00K
The following signals do not go to Max 10.
DBG_SWDIO, DBG_SWO, DBG_SWCLK

EFM32_JTAG_TCK
EFM32_JTAG_TMS
EFM32_JTAG_TDI
EFM32_JTAG_TDO
EFM32_RESETn
EFM32_INT
BLE_INT
SPI_SCLK
SPI_USB_CSn
SPI_MOSI
SPI_MISO
UART0_RX
UART0_TX
I2C_SCL
I2C_SDA
MAX10_I2C_SCL
MAX10_I2C_SDA

3.3V
ADC_REF
3V3_IN
VCCIO_B
J3 HDR 1X15
DIGITAL13
ANALOG_SIG1
ANALOG_SIG2
ANALOG_SIG3
ANALOG_SIG4
ANALOG_SIG5
ANALOG0
RESET
J4 HDR 1X15
DIGITAL12
LVDS_I_CLK_N
LVDS_I_CLK_P
LVDS_OUT3_N
LVDS_OUT3_P
LVDS_OUT2_N
LVDS_OUT2_P
LVDS_OUT1_N
LVDS_OUT1_P
LVDS_OUT0_N
LVDS_OUT0_P
CLK_RST
LVDS_O_CLK_N
LVDS_O_CLK_P

DIGITAL12
DIGITAL13
ANALOG0
ANALOG_SIG[1:5]
RESET
CLK_RST
LVDS_I_CLK_N
LVDS_I_CLK_P
LVDS_O_CLK_N
LVDS_O_CLK_P
LVDS_OUT3_N
LVDS_OUT3_P
LVDS_OUT2_N
LVDS_OUT2_P
LVDS_OUT1_N
LVDS_OUT1_P
LVDS_OUT0_N
LVDS_OUT0_P

3.3V
R17 10.0K PB0
R35 10.0K PB1
S1 PB-SPST-NO
S2 PB-SPST-NO

3.3V
LED0 D8 LED_RES0 R9 39.00 GREEN LED
LED1 D7 LED_RES1 R10 39.00 GREEN LED
LED2 D6 LED_RES2 R11 39.00 GREEN LED
LED3 D5 LED_RES3 R12 39.00 GREEN LED
LED4 D4 LED_RES4 R13 39.00 GREEN LED
LED5 D3 LED_RES5 R14 39.00 GREEN LED
LED6 D2 LED_RES6 R15 39.00 GREEN LED
LED7 D1 LED_RES7 R16 39.00 GREEN LED
IR_LED D9 IR_LED_RES R60 100 IR19-21C/TR8

LED[0:7]
IR_LED

Gain resistors (R46+R47)/R46 are placeholders,
still need to but shouldn't need any gain.

MIC_ANALOG_SIG = OPAMP_IN * OPAMP GAIN

MIC_PWR
C1 0.1uF 25V
U2 INMP404
VDD
OUTPUT
GND
MIC_OUT
C2 1uF 16V
C25 1uF 16V
R4 1.00K R1
R5 75K R2
GAIN = (R1 + R2)/R1
R3 10.0K
R7 0
OPAMP_IN_NEG
OPAMP_IN
U8 LT6220
MIC_ANALOG_SIG
R6 10.0K
Non-inverting pre-amplifier

2.5V
L2 BEAD
3.3V
L1 DNI

3.3V
R44 10.0K DIPSW0
R42 10.0K DIPSW1
R39 10.0K DIPSW2
R34 10.0K BOOT_SEL
SW1 SPST4
BOOT_SEL_PU
R36 1.00K
Max 10 HB recomends BOOT_SEL:
10K-ohm PD to select CFM0
10K-ohm PU to select CFM1 or CFM2
*Used a stronger PU since both resistors are in circuit when SPST ON.

PB[0:1]
DIPSW[0:2]
BOOT_SEL
CLK_50MHZ

3.3V
R38 10.0K CLK_EN
Y1 50MHz
EN
VDD
GND
CLK
50MHZ_OUT
R47 24.9
CLK_50MHZ
C7 0.1uF 25V
LAYOUT NOTES:
- Place 24.9 ohm resistor near oscillator.

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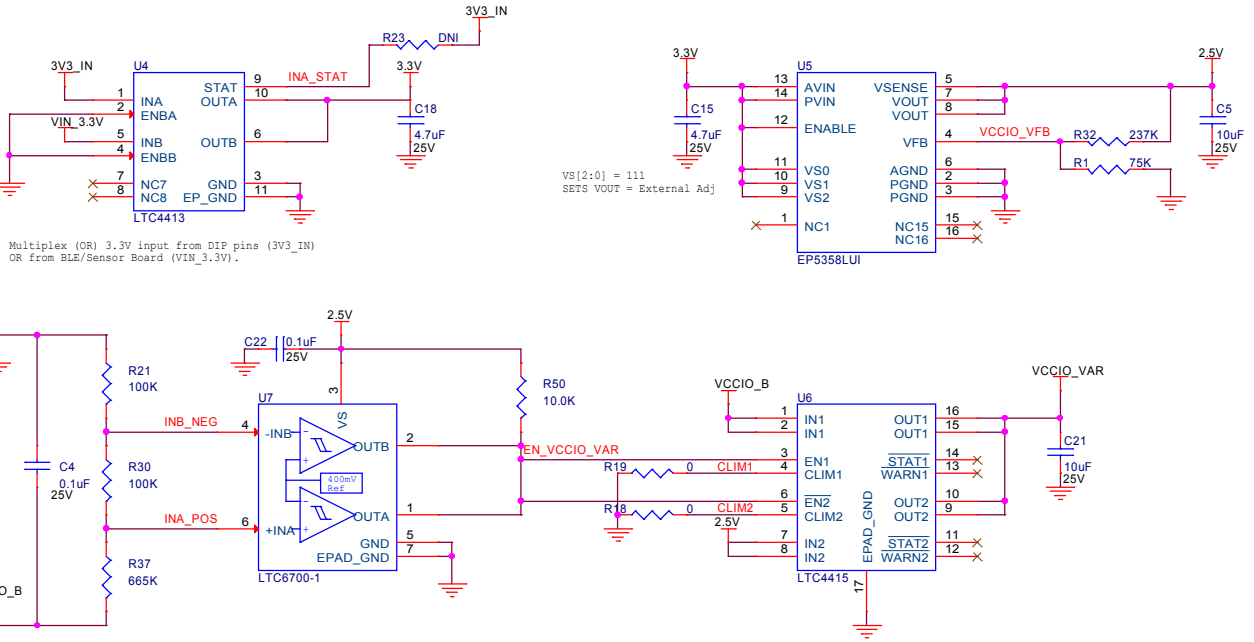
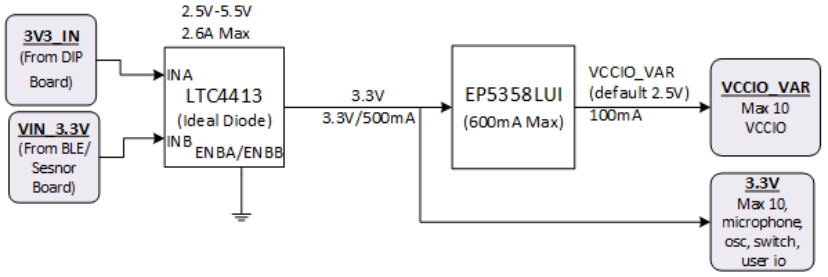
POWER

VCCIO_VAR power rail selection for Max 10.
- *2.5V (From EP5358LU)*
- *VCCIO_B = 1.8V - 3.3V (From DIP connector pins)*
- *VCCIO_VAR = VCCIO_B, unless not available then 2.5V*





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